In the Claims:

Please amend claims 1 and 2 as follows:

1. (currently amended) An improved voltage to current converter circuit in CMOSFET technology comprising:

- first and second input terminals to receive input voltage signals;

- an amplifying stage having first and second differential inputs connected to said first and second input terminals and first and second differential outputs;

- current source means biased between first and second supply voltages comprising a first current source generating a current connected to said first differential output loaded by a first transistor, and second/third current sources respectively generating current and connected to said second differential output loaded by a second transistor, wherein said transistors are connected in a current mirror mode with a common node therebetween;

- an output stage consisting of third and fourth transistors forming a half cascode current mirror having the drain of said third transistor connected to said second differential output and to the gate of the fourth transistor at a node forming the voltage to current converter circuit output terminal and having its gate connected to a bias voltage; and[[;]]

- variable bias means consisting of a fifth transistor, the drain of which is coupled to the gate of said third transistor and the gate is coupled to said common node.

2. (currently amended) The improved voltage to current converter circuit of claim1 wherein said ~~voltage~~ bias <u>voltage</u> is obtained from of a current source with a resistor connected in series therewith.